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Interfacing an EE-PROM with an 8-bit microprocessor

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With the advent of the 5-volt-only electrically erasable programmable read-only memory, single-board microcomputer systems that require nonvolatile memory no longer need a battery back-up circuit: with this circuit, Seeq Technology Inc.'s 2-K-by-8-bit EE-PROM can interface with RCA's 8-bit microprocessor CDP1802A. Although the EE-PROM's read time is fast, its write time is several magnitudes greater than the write time for a normal random-access memory.

The microprocessor's address bus is multiplexed with its timing pulse, TPA, latching the upper address lines, A_8–A_{15}, into latch U_3 (see figure). While A_0–A_{10} feed EE-PROM U_2, A_{11}–A_{15} drive decoder U_4, which selects the eight memory banks, all of them 2-K bytes apart.

The first output of the decoder, employed as an EE-PROM enable, is NORed with the memory-write signal provided by microprocessor U_1. So when a memory write is requested, NOR gate $U_{7\text{-}a}$'s output goes from low to high and clocks flip-flop U_{11}. This enables the flip-flop's $\overline{Q}$ output to generate a low wait pulse that when fed to the microprocessor causes all output lines to freeze in their current state. Also, $U_{7\text{-}a}$'s output simultaneously initiates presettable down-counters U_9 and U_{10}, enabling U_9, which is clocked by U_8's output, to generate a negative-going pulse every 200 microseconds. Counter U_{10} counts these pulses for a period of 1.2 milliseconds.

U_{10}'s output resets U_{11} at the end of 1.2 ms and clears the wait timing condition. For the processor to respond to this condition, it is necessary to use a faster microprocessor, such as CDP1802A.

A 470-ohm pull-up resistor connected to the EE-PROM's write-enable pin stops false write-up when the power is switched on. This resistor also acts as the pull-up for bilateral switch U_{12}, used in a pseudo–open-collector mode. So when the +5-V supply falls below 4.5 V, inverter $U_{5\text{-}f}$'s output goes high and the associated logic prevents premature memory write. □

Interface. This circuit links RCA's 8-bit microprocessor CDP1802A with Seeq's 5-volt-only electrically erasable PROM 5213H and provides the system with nonvolatile memory that needs no battery backup. Address lines A_0 through A_{10} feed the EE-PROM, while A_{11} through A_{15} drive decoder U_4. The first output of this decoder covers the memory address 0000_{16}–$07FF_{16}$. It also the EE-PROM–enable pulse that is NORed with the memory-write signal generated by the processor. As a result, the logic generates a 1.2-ms wait pulse, which freezes all output lines when a memory write is requested.